2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Suppl. 4/B

In re application of

WILLIAM P. STEARNS ET AL.

Serial No. 09/678,318 (TI-25833.1)

Filed October 3, 2000

For: OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

Art Unit 2814

Examiner

Commissioner for Patents
Washington, D. C. 20231

Sir:

SECOND PRELIMINARY AMENDMENT

Prior to the first Office action, please amend the Abstract as follows:

" A method of laying out traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like and the layout. There is provided a substrate having top and bottom surfaces with a plurality of rows and columns of vias extending therethrough from the top surface to the bottom surface and having a solder ball secured at the surface of each via. A plurality of pairs of traces is provided on the top surface, each trace of each pair of traces extending to a different one of the vias and extending to vias on a plurality of rows and columns, each of the traces of each pair being spaced from the other trace by a ball pitch, being maximized for identity in length and being maximized for parallelism and spacing. Each of the traces of a pair is preferably [be]